Petronela BONTEANU

INFORMAȚII PERSONALE

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Sex F | Data nașterii 25/06/1982 | Naționalitate Română

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EDUCAȚIE

2018 - Prezent

Doctorat

Universitatea Tehnică ”Gheorghe Asachi” Iași, Școala Doctorală

- Dezvoltarea interfețelor om-masină bazate pe detecția direcței privirii
  Îndrumător: Prof.Dr.Ing. Bozomitu Radu Gabriel

2005 - 2006

Master

Universitatea Tehnică ”Gheorghe Asachi” Iași, Facultatea de Electronică şi Telecomunicaţii

- Inginerie Biomedicală, " Proiectarea si implementarea unui oscilator haotic”
  Îndrumător: Prof.Dr.Ing. Horia-Nicolai Teodorescu

2005 : 03->06

ERASMUS

Institut Politechnique de Grenoble ESISAR-LCIS

2000 - 2005

Inginer diplomat

Universitatea Tehnică ”Gheorghe Asachi” Iași, Facultatea de Electronică şi Telecomunicaţii

Comunicaţii, “Proiectarea si implementarea unui transceiver UWB pentru domeniul 3.1-10.6GHz”
Îndrumător: Prof.Dr.Ing. Duma Petruț

EXPERIENȚĂ PROFESIONALĂ

2009 -2019

Backend ASIC designer

SC Silicon Service SRL

- - Power Analysis, DRC/LVS checks

Sector Industrie

2008 - 2009

Circuit designer

SC Asic Art SRL for IBM

- -Schematic design, netlist (spectre,spice), post layout simulations , layout design, DRC, LVS, PEX checks

Sector Industrie

2005 - 2008

Circuit designer

SC Asic Art SRL

- -Schematic design, netlist (spectre,spice), post layout simulations , layout design, DRC, LVS, PEX checks

Sector Industrie

ABILITĂȚI PERSONALE

Limba maternă: Română

Alte limbi

	ÎNȚELEGERE		VORBIRE		SCRIERE
	Ascultare	Citire	Participare la conversație	Discurs oral	
Engleză	B2	B2	B1	B1	B2
Franceză	A2	A2	A2	A2	A2
Germană	A1	A1	A1	A1	A1

Competențe și abilități sociale

- Spirit de echipă pronunțat

Competențe și aptitudini organizatorice

- Bun spirit organizatoric

Competențe și aptitudini tehnice

- **Analog projects:**
- Serializer / Deserializer TSMC 90/180 nm technology -layout design (from standard cells to top level) , DRC/LVS checks.
- Electronically-programmed fuses (128-bit eFuse)-1.65V–1.95V (VDD range)-Layout Migration from CMOS7RF to BICMOS7HP 90nm technology, collaboration with IBM Company -DRC/LVS checks.
- Custom circuit SOM Design (Shorts & Opens Monitor) - 22nm IBM technology using SKILL scripts for Fab's process testing.
- VRL (Voltage Linear Regulator) - 1.8V output ± 5% ,120mA/80mA maximum Load current; Migration from SMIC 180nm technology to Tower 180nm low-leakage technology -schematic (PVT tests), layout design and DRC/LVS checks ; collaboration with MOSCAD-DA company.
- LDO (Linear Drop-Out voltage) - 1.8V output ± 5%,400mA maximum Load current; Overload protection trough current limiting. Maximum load regulation drop of 50mV. Migration from SMIC 180nm technology to Tower 180nm low-leakage technology -schematic (PVT tests), layout design and DRC/LVS checks.
- POR (Power-on Reset) 3.3V power supply reset, 1V minimum operating Voltage, 11µA Total Current Consumption, glitch detection/rejection, build in hysteresis. Migration from SMIC 180nm technology to Tower 180nm low-leakage technology - schematic (PVT tests) and layout design and DRC/LVS checks.
- VCO -Voltage Controlled Oscillator-schematic (PVM tests) and layout in UMC 180nm technology.
- PLL(Phase Locked Loop) at 1.4 GHz (layout) in UMC 180nm technology.

- **Digital projects:**
- Digital standard cells design -layout in different technologies.
- Digital block on MagnaChip 350nm technology , 4 metal layers , ~ 45000 gates -Power Analysis, DRC/LVS checks.
- Digital block including IO cells on MagnaChip 350nm technology, 4 metal layers ,~ 16000 gates, Power Analysis, DRC/LVS checks.
- Digital block - on Atmel 350nm technology , 3/4 metal layers - DRC/LVS checks.

- **Verilog training projects :**
- Am2910A - bit-slice microprogram address sequencer for controlling the sequence of execution of

microinstructions stored in microprogram memory.
- FIFO asynchronous
- Router with a configurable number of bidirectional channels.
- PWM (pulse width modulation) generator with changeable frequency and duty-cycle.

Competențe și aptitudini de utilizare a calculatorului

- IBM -in-house verification suite, Cadence Custom IC package, Cadence Soc Encounter, Synopsys HSpice, Mentor Graphics-Calibre, Cadence Assura, Synopsys Hercules, Mentor Graphics - ModelSim, Matlab, Python;

Proiecte de cercetare

- **COMPETE 2.0 - PN III 27PFE/2021**

Lucrări stiințifice

- Bonteanu, G.; **Bonteanu, P.**; Cracan, A.; Bozomitu, R.G. Implementation of a High-Accuracy Neural Network-Based Pupil Detection System for Real-Time and Real-World Applications. **Sensors 2024**, 24, 2548. https://doi.org/10.3390/s24082548
- **P. Bonteanu**, A. Cracan, Gabriel Bonteanu, Radu Gabriel Bozomitu, A New Robust Pupil Detection Algorithm for Eye Tracking Based Human-Computer Interface, International Symposium on Signals, Circuits and Systems, ISSCS 2019, Iasi, Romania
- **P. Bonteanu**, Arcadie Cracan, Gabriel Bonteanu, Radu Gabriel Bozomitu, A High Detection Rate Pupil Detection Algorithm Based on Contour Circularity Evaluation, 2019 IEEE 25th International Symposium for Design and Technology in Electronic Packaging (SIITME), Cluj-Napoca, Romania
- **P. Bonteanu**, Arcadie Cracan, Gabriel Bonteanu, Radu Gabriel Bozomitu, A New Pupil Detection Algorithm Based on Circular Hough Transform Approaches, 2019 IEEE 25th International Symposium for Design and Technology in Electronic Packaging (SIITME), Cluj-Napoca, Romania
- **P. Bonteanu**, Arcadie Cracan, Gabriel Bonteanu, Radu Gabriel Bozomitu, A Robust Pupil Detection Algorithm Based on a New Adaptive Thresholding Procedure, IEEE International Conference on e-Health and Bioengineering EHB 2019, Iasi, Romania
- **P. Bonteanu**, Radu Gabriel Bozomitu, Arcadie Cracan, Gabriel Bonteanu, „A Pupil Detection Algorithm Based on Contour Fourier Descriptors Analysis", 2020 IEEE 26th International Symposium for Design and Technology in Electronic Packaging (SIITME)
- **P. Bonteanu**, Radu Gabriel Bozomitu, Arcadie Cracan, Gabriel Bonteanu, A New Pupil Detection Algorithm Based on Multiple Angular Integral Projection Functions, EHB 2021
- Gabriel Bonteanu, **P. Bonteanu**, Arcadie Cracan, Radu Gabriel Bozomitu, A New Hybrid Pupil Detection Algorithm for Real Time Applications, EHB 2023
- Gabriel Bonteanu,**P. Bonteanu**, Arcadie Cracan, Radu Gabriel Bozomitu, Implementation of a high accuracy pupil detection algorithm using neural networks, SIITME 2023
- ICDS 2023 – "Neural network classifier based gaze detector", G. Bonteanu, **P. Bonteanu**, A. Cracan, R. G. Bozomitu;
- ICDS 2024 – " Enhancing Vehicle Assembly with AI-driven Gaze Detection in Augmented Reality Systems", **P. Bonteanu** G. Bonteanu

Brevete

- METODA PENTRU REDUCEREA COSTURILOR IMPLEMENTĂRII CLASIFICATOARELOR BAZATE PE TEHNOLOGIA REȚELELOR NEURONALE UTILIZATE ÎN DETECȚIA PRIVIRII, A/00586 20.10.2023

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- 17 times cited

ResearchGate

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